



# SUPERMICRO HYPER SERVERS DEMONSTRATE HIGH PERFORMANCE RUNNING A RANGE OF EDA BENCHMARKS

*Supermicro Servers Show Increased Performance Per Watt with High-End 4<sup>th</sup> Gen AMD EPYC™ Processors*



Figure 1 - Supermicro Hyper System – AS -2115HS-TNR

## Executive Summary

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Electronic Design Automation (EDA) encompasses a suite of software tools that automate the design and analysis of electronic systems, such as integrated circuits and printed circuit boards. These tools streamline the design process by enabling engineers to create complex circuits, simulate their behavior, verify their functionality, and optimize their manufacturing, ultimately accelerating the development of innovative electronic devices while minimizing design errors

and reducing time-to-market. Supermicro servers excel at running these applications across a range of 4<sup>th</sup> Gen AMD EPYC™ processors. Several tests were run on software from several Supermicro Hyper AS -2015HS-TNR system vendors. The AS -2015HS-TNR consisted of a single 4<sup>th</sup> Gen AMD EPYC 9654 processor and 1.5TB of DDR5-4800 of memory.



## Benchmark Description

The following benchmarks were run on a variety of 4<sup>th</sup> Gen AMD EPYC CPUs. The tests were simulating an internal AMD CPU design.

**Synopsys VCS** - The Synopsys VCS® functional verification solution is the primary verification solution used by a majority of the world's top semiconductor companies. VCS provides the industry's highest-performance simulation and constraint solver engines. VCS' simulation engine natively takes full advantage of multicore processors with state-of-the-art Fine-Grained Parallelism (FGP) technology, enabling users to easily speed up high-activity, long-cycle tests by allocating more cores at runtime.

**Synopsys Fusion Routing** - Synopsys Fusion Compiler™ serves as a unified tool designed for Register Transfer Level to Graphic Data System version II (RTL-to-GDSII) implementation. This comprehensive and integrated design and implementation environment combines advanced optimization algorithms with low-power design techniques and support for advanced process nodes. Its primary objective is to facilitate efficient and highly performant integrated circuit designs.

**Siemens Tessent** - Siemens Tessent is a software tool suite that helps design and test integrated circuits (ICs). It focuses on improving the testability of chips, accelerating manufacturing yields, and enhancing their overall quality and reliability. This is achieved through features like Design-for-Test (DFT) solutions, manufacturing test solutions, and in-system test solutions, ultimately ensuring that the produced chips function correctly and meet the highest quality standards.

**Siemens Calibre** - Siemens Calibre is a suite of software tools crucial for verifying the accuracy and manufacturability of integrated circuits (ICs). It performs checks like Design Rule Checks (DRC) and Layout vs. Schematic (LVS) and analyzes for potential reliability issues. This ensures chip designs are free from errors, optimized for production, and ultimately improve the success of the chip development process.

**Cadence SpectreMX (NUMA)** - Cadence Spectre MX is a high-performance circuit simulator within the Cadence Spectre family, designed for mixed-signal integrated circuits. It strikes a balance between simulation speed and accuracy, making it suitable for efficiently simulating complex circuits while maintaining reliable results. This helps engineers accelerate the design process and improve overall design quality.

**Synopsys PrimeSim** - Synopsys PrimeSim is a suite of circuit simulation tools that enables efficient and accurate analysis of integrated circuits. It integrates various simulation engines, offers high performance, and supports a wide range of analyses, helping engineers accelerate the development process and improve the quality of their chip designs.

**Synopsys Fusion Synthesis** - Synopsys Fusion Compiler is a revolutionary new IC design tool that integrates synthesis and place & route, breaking down traditional barriers in the design flow. This unified approach leads to significant improvements in power, performance, and area (PPA) while accelerating the design process and improving predictability.

**Synopsys Formal** - Synopsys Formal is a suite of tools that uses advanced mathematical techniques to verify the correctness of integrated circuit designs rigorously. Finding and fixing bugs early in the design process significantly increases design confidence and reduces the risk of costly failures.

**Ansys Redhawk-SC** – Ansys Redhawk-SC is a leading software tool for power integrity and reliability signoff in the semiconductor industry. It accurately predicts power supply noise, electromigration, and other reliability issues in complex ICs, ensuring their correct and reliable operation in real-world conditions.

## Test System Configuration

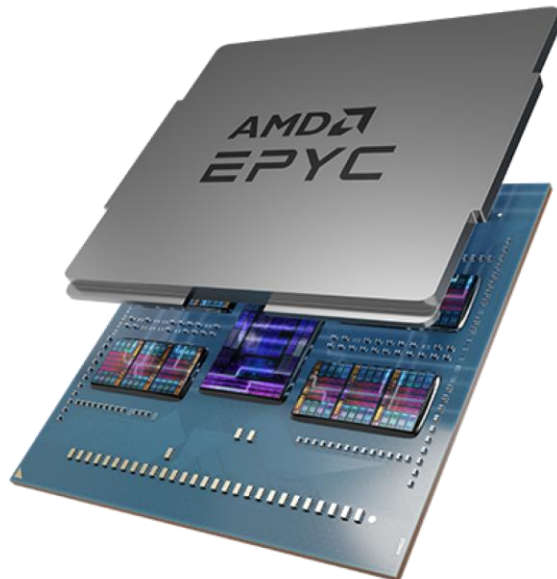
The test system for all of these tests was:

- Supermicro Hyper System – AS -2115HS-TNR
  - Various AMD EPYC CPUs
  - 1.5TB of DDR5-4800 Memory
  - 1.9TB NVMe Storage

There are a number of 4<sup>th</sup> Gen AMD EPYC CPUs that were tested. Specifically:

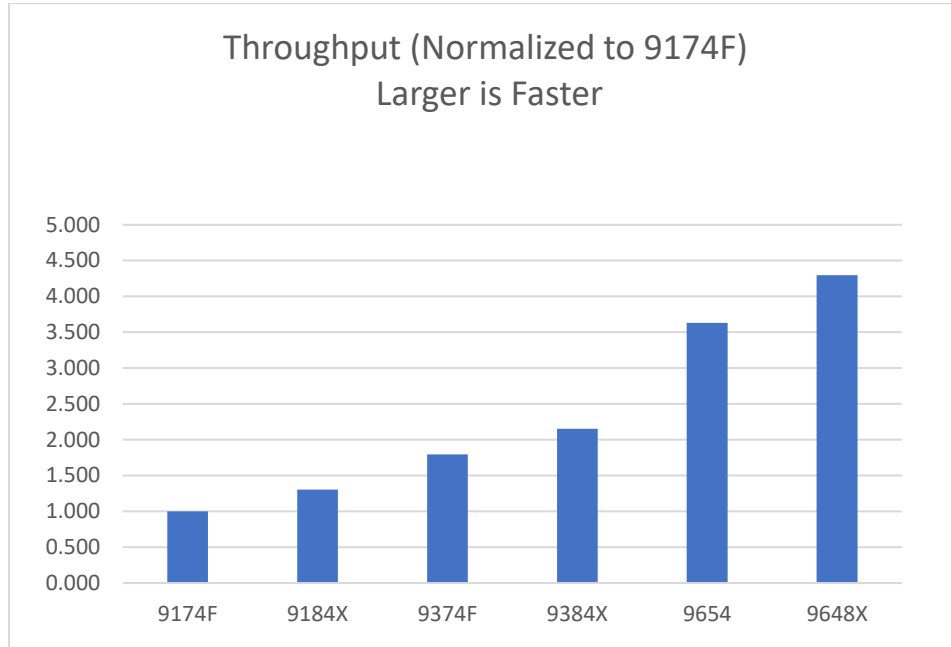
AMD EPYC Processor	Cores/Threads	Base Frequency (GHz)	TDP (Watts)
9174F	16 / 32	4.10	320
9184X	16 / 32	3.55	320
9374F	32 / 64	3.85	320
9384X	32 / 64	3.10	320
9654	96 / 192	2.40	360
9684X	96 / 192	2.55	400

The “X” designation in the Processor SKU refers to AMD 3D V-Cache technology.

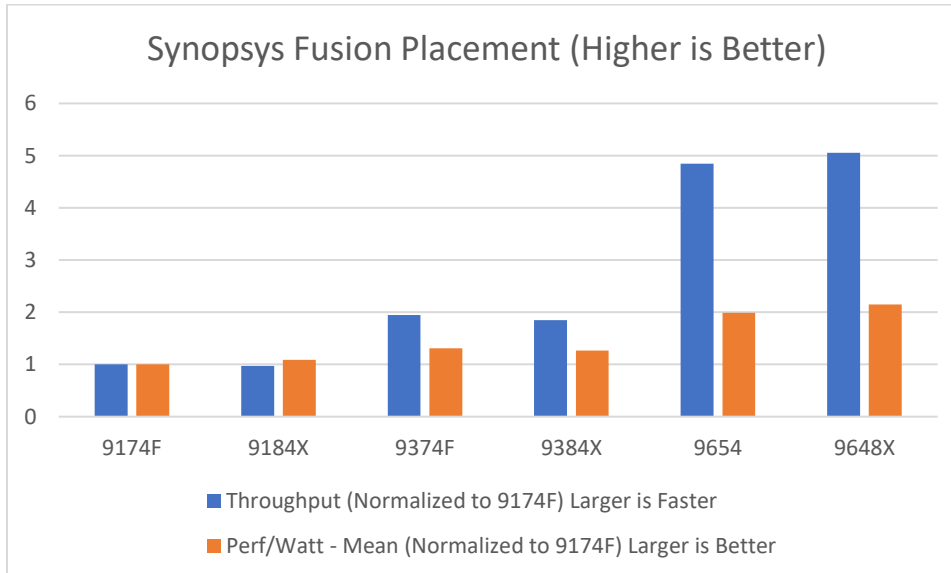


## Test Results

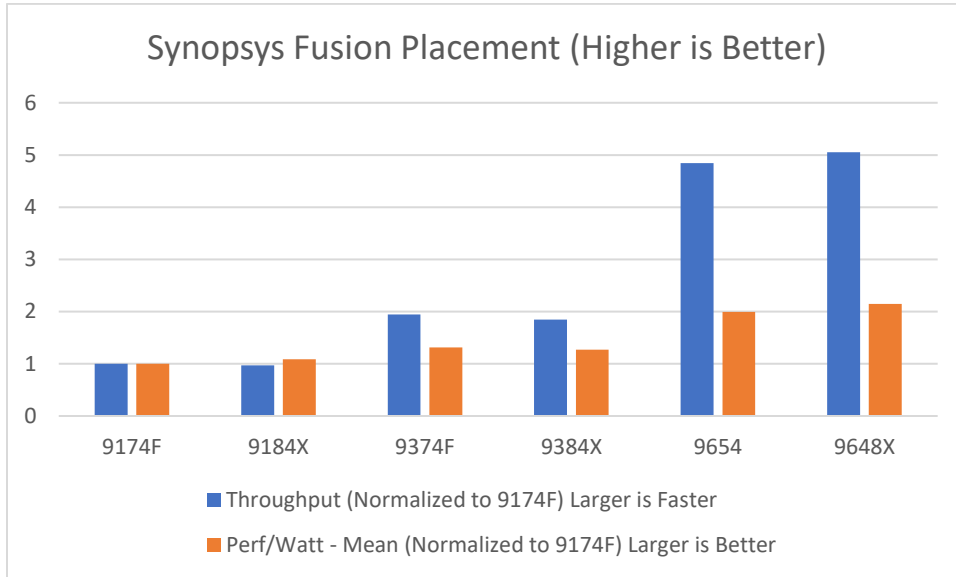
### 1) Synopsys VCS



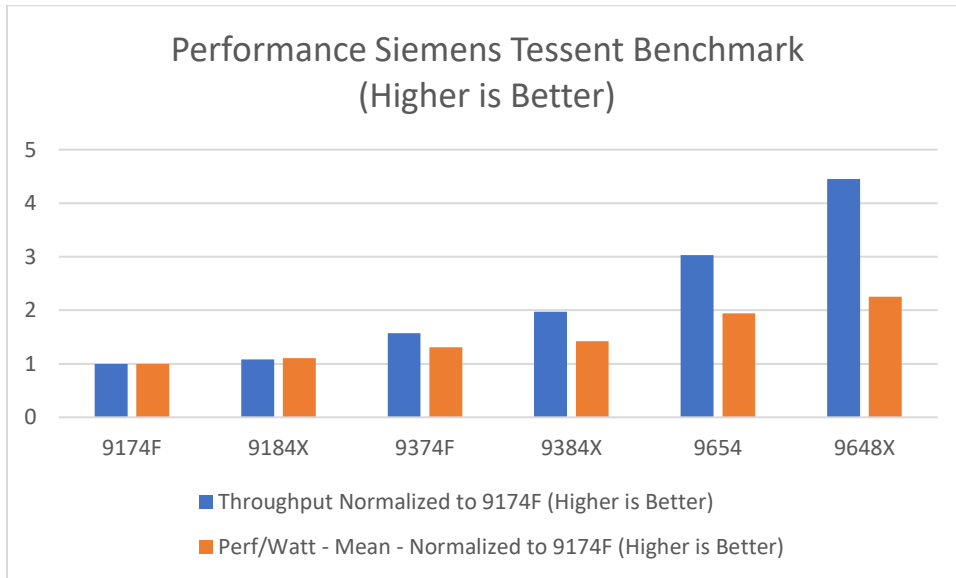
### 2) Synopsys Fusion Placement



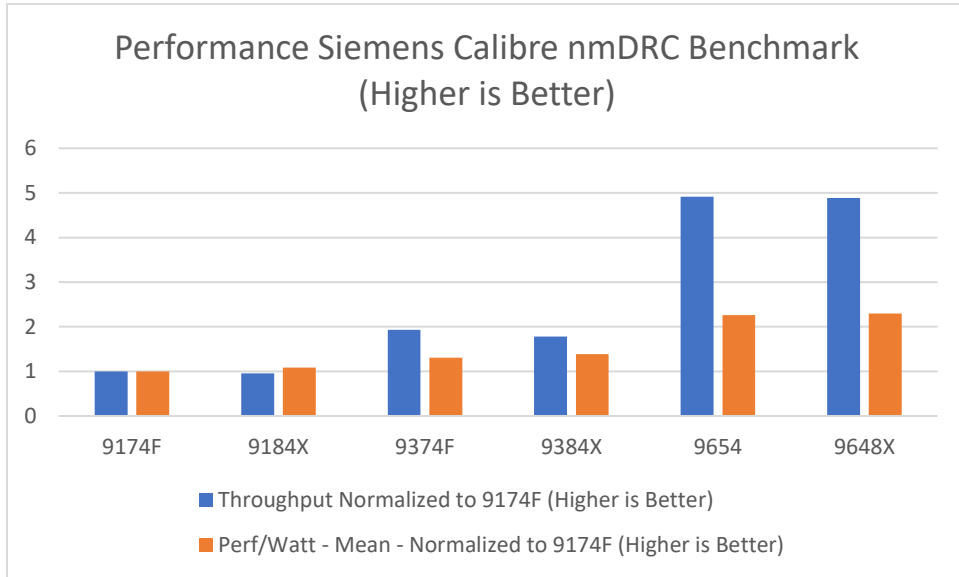
### 3) Synopsis Fusion Routing



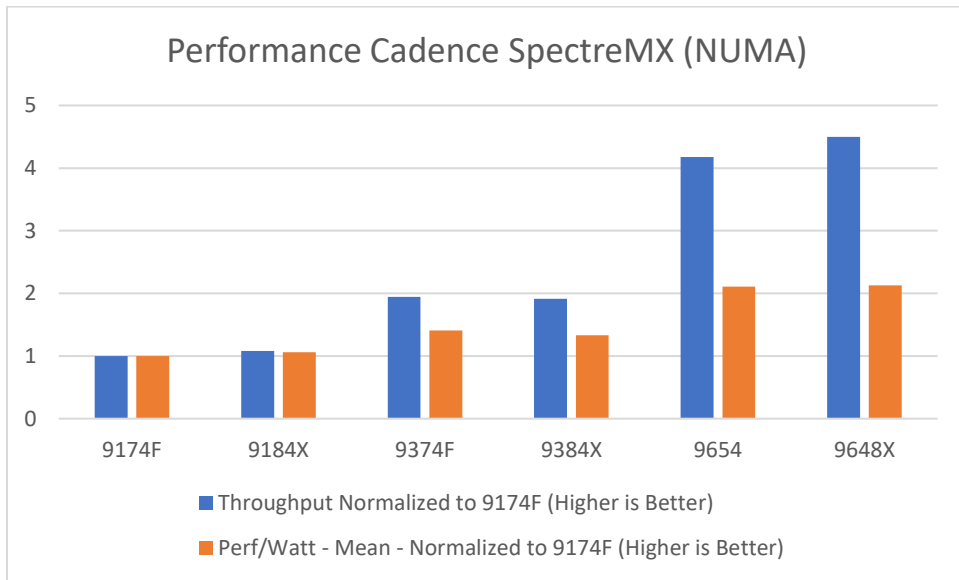
### 4) Siemens Tessent



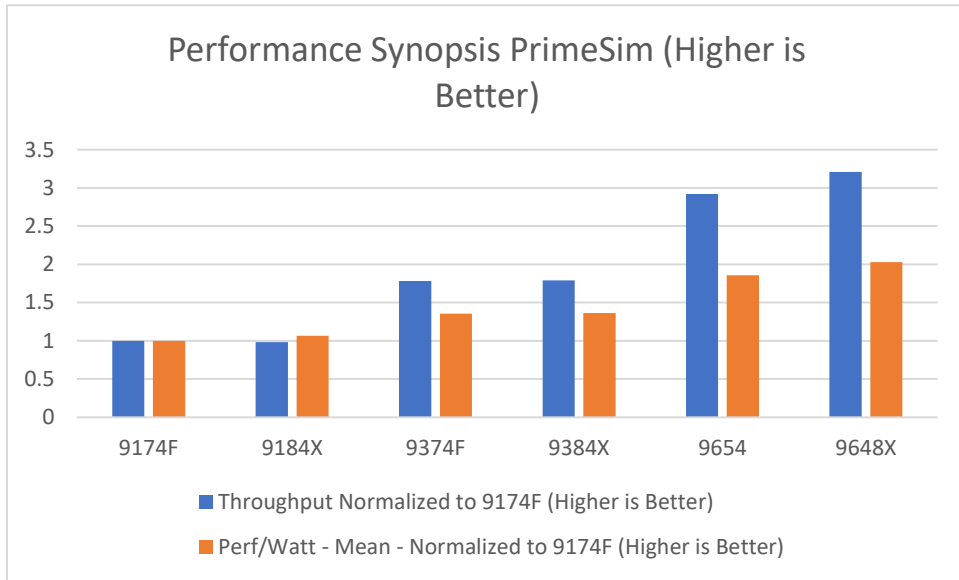
5) Siemens Calibre nmDRC



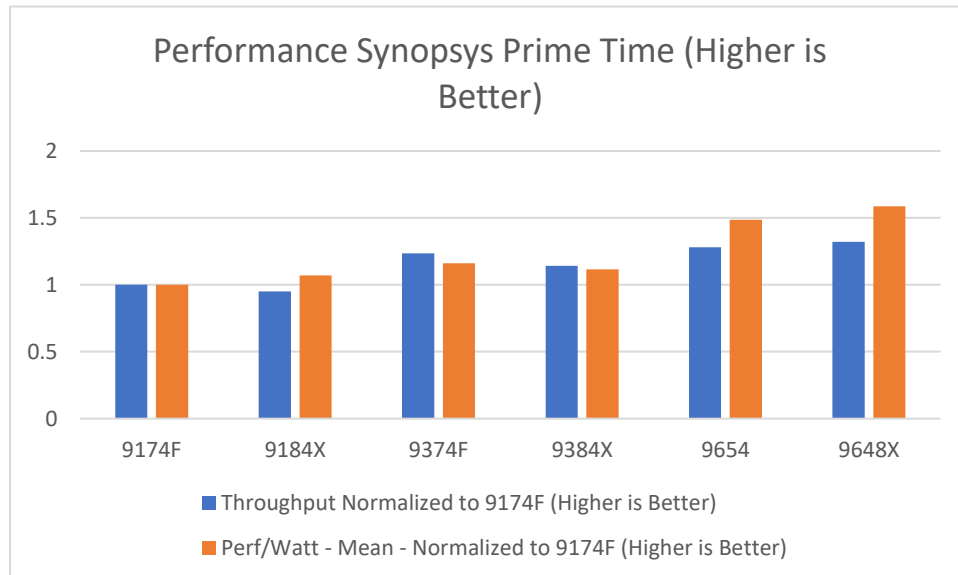
6) Cadence SpectreMX (NUMA)



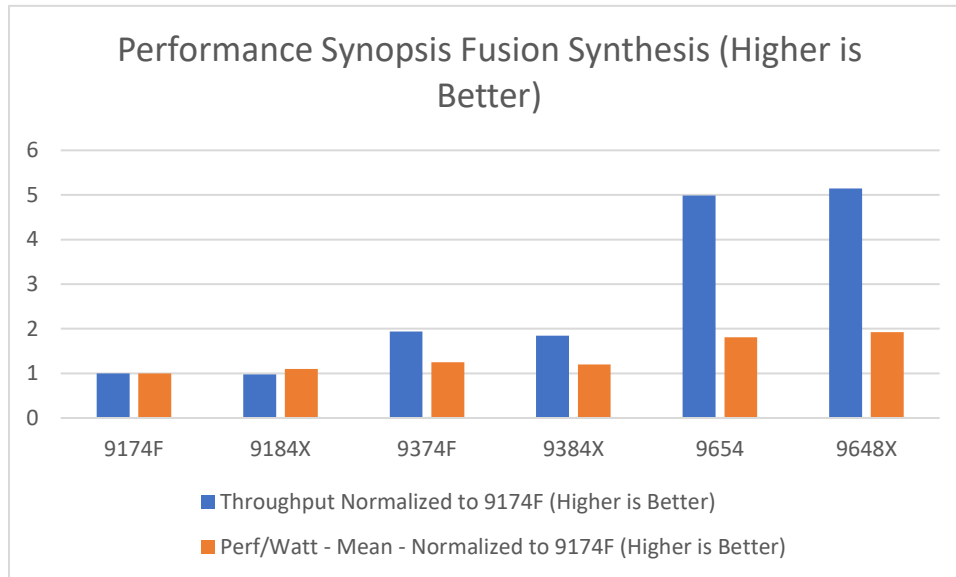
7) Synopsis PrimeSim



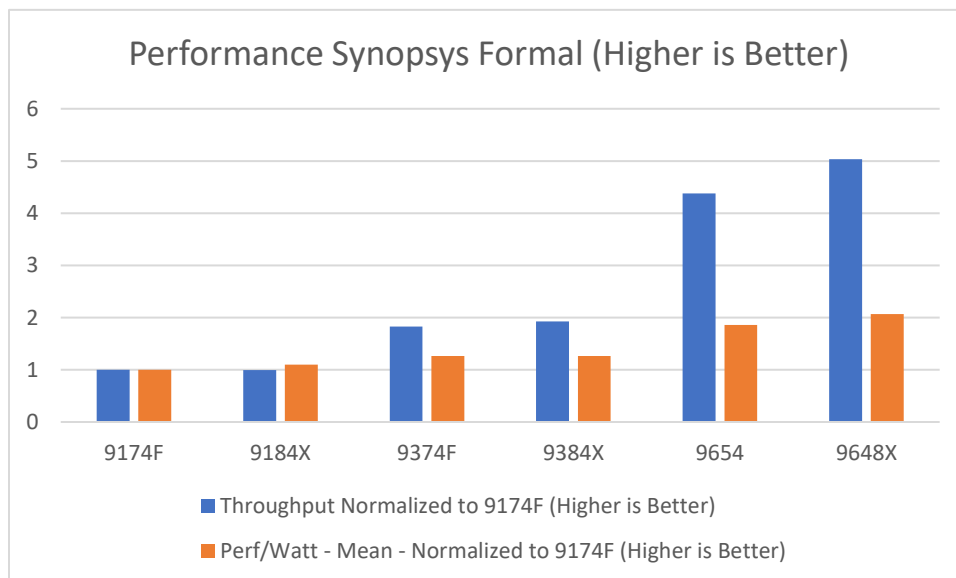
8) Synopsis PrimeTime



## 9) Synopsys Fusion Synthesis

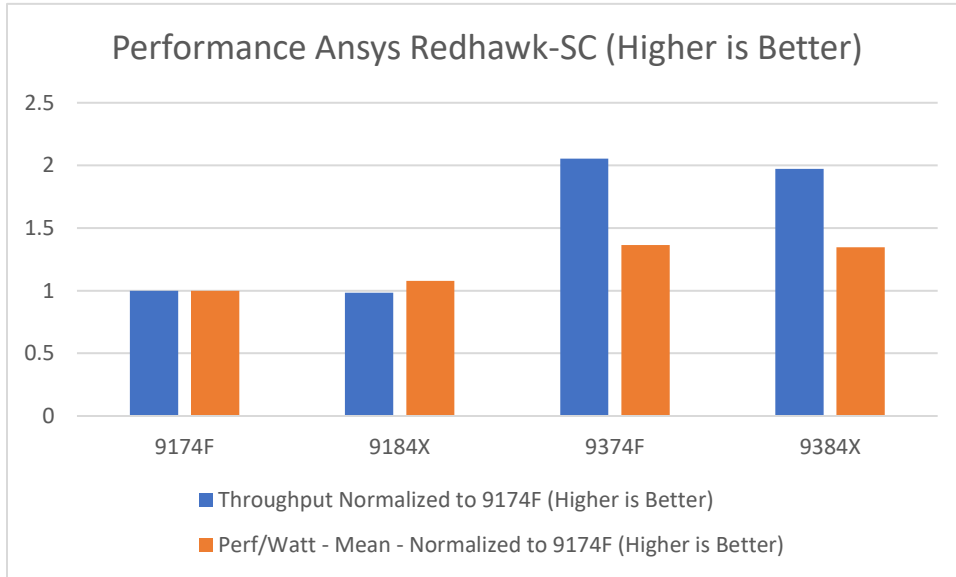


## 10) Synopsys Formal





## 11) Ansys Redhawk-SC



### Summary

The Supermicro Hyper server, the AS -2115H-TNR, demonstrates high-end performance when running various EDA benchmarks. The throughput of each application was measured on different AMD EPYC CPUs, and the performance increased as the number of cores per CPU increased—also, the efficiency increased by measuring the performance per watt as the higher-end processes were used.

### For more information:

Supermicro Hyper Product Family: <https://www.supermicro.com/en/products/hyper>

AMD Document on EDA Results:

[https://www.amd.com/en/search/documentation/hub.html?q=EDA%20Benchmarks&sortCriteria=%40amd\\_release\\_date%20descending&f-amd\\_document\\_type=Performance%20Briefs&f-amd\\_product\\_series=EPYC%209004%20Series](https://www.amd.com/en/search/documentation/hub.html?q=EDA%20Benchmarks&sortCriteria=%40amd_release_date%20descending&f-amd_document_type=Performance%20Briefs&f-amd_product_series=EPYC%209004%20Series)

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